CERN
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1981.02.12

SYSTEM ENCODER TYPE 158

TECHNICAL SPECIFICATIONS

The System Encoder (SE) is designed to control the read-out of a chain of crate encoder modules[1] (CE), types 7236 or 7236A, connected to the vertical dataway (branch). It receives data from the branch via the branch input connector* or the internal input bus in strobed mode (format, see Fig. 1), encodes each hit wire of the data pattern into a binary address, merges crate and station address from CE into a contiguous station address and adds the flag bit (if present) to the first encoded hit wire (format, see Fig. 2). The function of SE itself is controlled via an external device (ED), for ex.: the CAMAC interface[2] (IF), type 159, or processor via a fan-out[3] (FO), type 180, connected to the internal output bus or to the data output connector**. See block diagram, Fig. 3. The conversation with the ED uses double handshake mode (see Fig. 4). A NIM output provides a signal (BUSY) indicating the complementary status. A control signal (ENFS) enables all CEs within a system to commence the preparation for data transfers from the first RMH module containing data within each crate, either via the start read signal (SR) from the ED or via the back edge of the fast strobe signal from the control unit module[4] (CU), type 9294, depending on the position of the start switch - external device or crate intern***.

The enable input signal (EI) enables the CEs to gate their data pattern, station address and crate address onto the branch. A rear input connector (NIM level) provides for an external reset to the SE, this also resets data in RMHs and CEs.

Examples for the extension of the basic system to a multi-branch and/or multi-output systems can be found in refs. 1 and 5. These options can be also implemented at a later stage. An assembled system (with options) represents a compact multi-module plug-in unit**** which - in general - will be inserted into a standard CAMAC crate.

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*) Note: The branch input connector shall not be used in a multi-branch configuration which uses the internal input bus.
**) Note: The data output connector shall not be used in a multi-output configuration which uses the internal output bus.
***) Note: If the position "crate intern" of the start switch is used a hang-up condition may occur if the crates are not strobed.
****) Note: Individual units cannot be extracted from this plug-in without extraction of the whole plug-in from the crate.

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1. INPUT

1.1 Branch Input connector (BI): p.c.b. edge connector, 2x35 contacts, $^1/_{10}$" pitch; ECL signals (single ended driven, other wire of pair statically at -1,4 V);
Connections: see Fig. 5.

1.2 Internal Input Bus connector (IIB)*: 2x40 contacts (2x2x20 headers); ECL signals (single ended driven, other wire of pair statically at -1,4 V; EIF and EO are driven push-pull).
Connections: see Fig. 6.

1.3 Branch termination: All branch signals are terminated with appropriate resistors inside module.

2. OUTPUT

2.1 Data Output connector (DO): p.c.b. edge connector, 2x35 contacts, $^1/_{10}$" pitch; ECL signals (complementary).
Connections: see Fig. 7.

2.2 Internal Output Bus connector (IOB)**: receptacle (female) for headers, 2x20 contacts: ECL signals (single ended driven, other wire of pair statically at ground).
Connections: see Fig. 8.

3. CONTROL

3.1 Front panel:

3.1.1 BUSY output: complementary NIM signal, false (0 Volts) if unit is busy; if used must be terminated with 50 Ω.

3.1.2 BUSY indicator: indicates status, "ON" when BUSY.

3.1.3 Start switch: toggle switch, 2 positions:

- crate intern (CRATE INT.)
- external device (EXT. DEVICE)

Enables the preparation for the first data transfer to the external device (ED) via either the start read signal from ED or the trailing edge of the common strobe from the CU within each crate.

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*) Option: only used in multibranch configuration.
**) only used if ED is connected to IOB.

3.2 Rear panel:

3.2.1 Reset input: NIM signal, internally terminated (50 Ω), min. width = 10 nsec: resets SE logic, all CEs and RMHs in system.

4. DATAWAY CONNECTIONS: (rear p.c.b. connectors, 2x43 pins, $^1/_{10}$" pitch).

No connections to dataway except for power supply and ground connections (see Fig. 9).

REMARK:

Unit may be inserted either in RMH-crate*** or in a standard CAMAC crate.

5. MECHANICS: CAMAC mechanics, 2 units wide.

6. POWER SUPPLY: -5,2 V/4,5 Amps or -6 V/4,5 Amps.

***) Remark: If interface (IF) connected to IOB, unit must be inserted in CAMAC crate.

REFERENCES

1. J.B. Lindsay, C. Millerin, J.C. Tarle, H. Verweij and H. Wendler, A fast and flexible data acquisition system for multiwire proportional chambers and other detectors, Proceedings of the Wire Chamber Conference, Vienna, Nuclear Instruments and Methods, 156 (1978).

2. H. Wendler, Interface, type 158, Technical specifications, CERN, EP Division (1979).

3. H. Wendler, Fan-out, type 180, Technical specifications, CERN, EP Division (1979).

4. J.C. Tarle, H. Verweij, Control unit, type 9294, Technical specifications, CERN, EP Division (1976).

5. J.C. Tarle and H. Wendler, Short description of the RMH-system, CERN, EP Division (1979).

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1979.05.01
Revised: 1981.02.12

LIST OF ABBREVIATIONS

BI	Branch input
BO	Branch output
BR	Branch receiver (module)
BT	Branch terminator (plug)
B0	Bit 0
B4	Bit 4
CE	Crate encoder (module)
CL.1	Clock 1 (internal)
CI	Chamber interface (module)
C0	Crate Address bit 0
DF	Device flag (handshake signal, response)
DO	Data output
ECL	Emitter coupled logic
ED	External device
EI	Enable input ("daisy" chain signal)
EIF	Enable input "first" (signal to "first" crate encoder)
ENC	Encode (handshake signal; request)
ENCSE	Encode from system encoder
ENFS	Enable fast strobe
EO	Enable output ("daisy" chain signal)
EOR	End of read-out (end of record)
ERR	Error
F	Flag bit
FF	Flip-flop (bistable)
FO	Fan out (module)
IF	Interface (module)
IIB	Internal input bus
IOB	Internal output bus
IRR	Initialise re-read
LC	Level converter (module)
LH	Lower half (of data pattern)
LSB	Least significant bit
MOR	Memory OR
MSB	Most significant bit
OP	Operational
PAR	Parallel
p.c.b.	Printed circuit board (p.c. board)
RD	Read
RMH	Receiver & memory on hybrid
RT	Reset
SE	System encoder (module)
SR	Start read system encoder (module)
S0	Station address bit 0
UH	Upper half (of data pattern)
WCI	Wire chamber interface (module)
W0	Wire number 0 (uncoded)

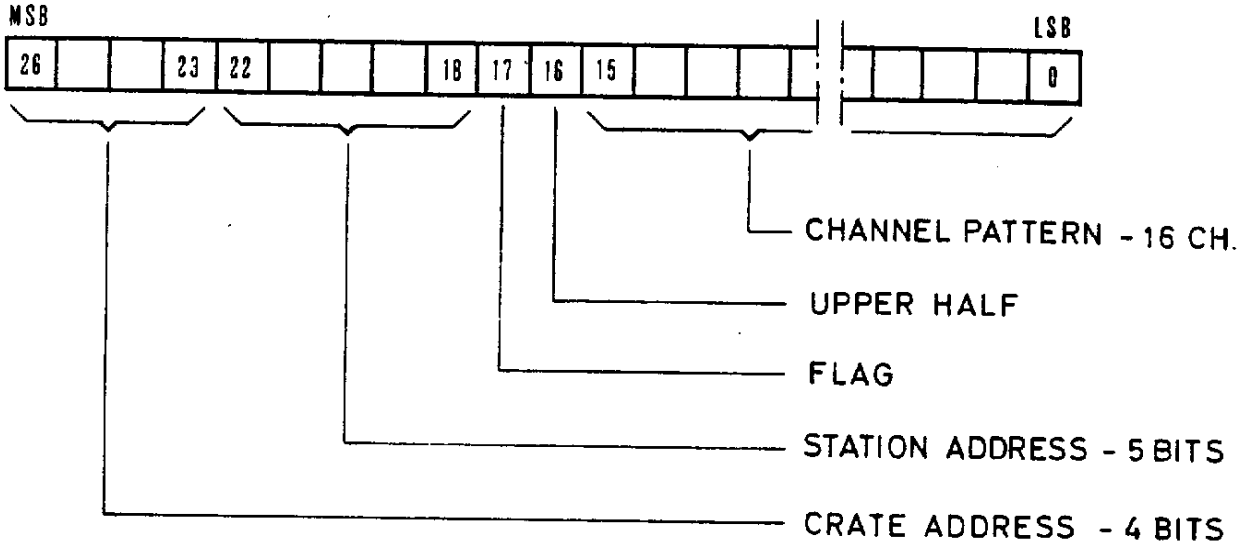

Fig. 1 BRANCH FORMAT

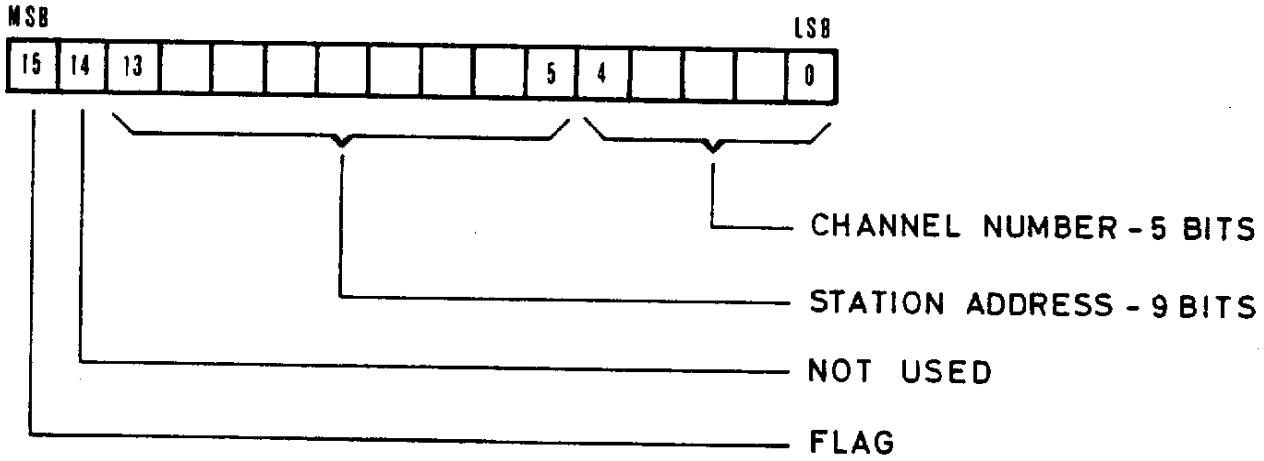

Fig. 2 BINARY FORMAT

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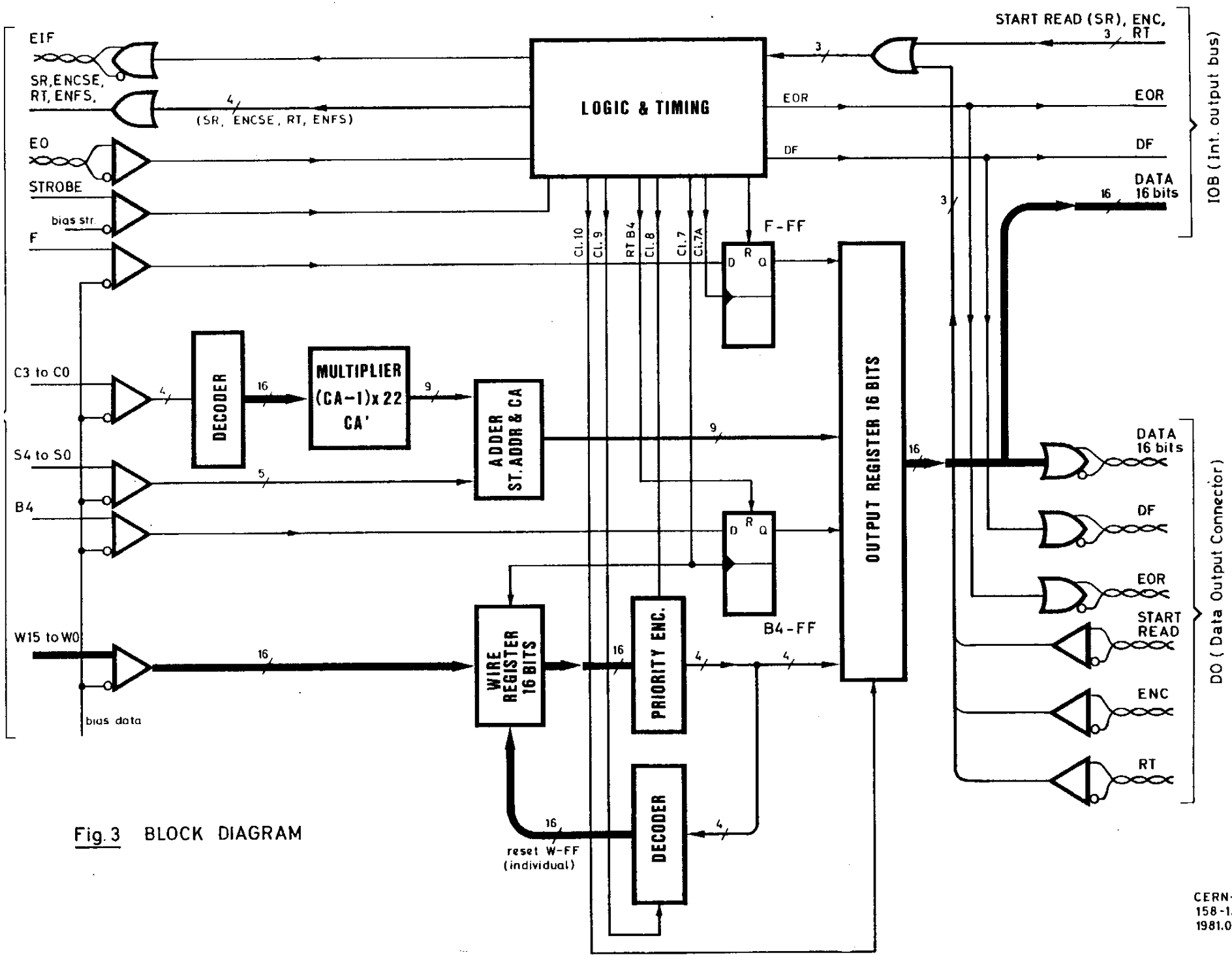

Fig. 3 BLOCK DIAGRAM

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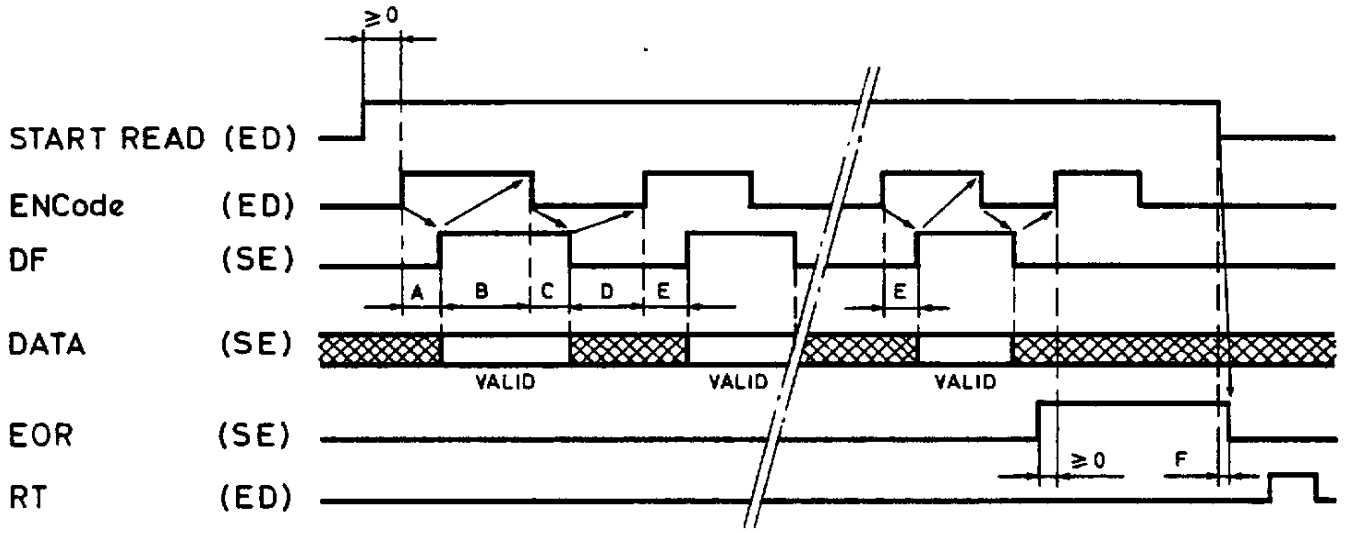

(ED) : External Device

(SE) : System Encoder

TIMES (typical) :

A	~	180 ns
B		dependant of ED (+ int. 20 ns)
C	~	30 ns
D		dependant of ED (+ int. 20 ns)
E	~	120 ns
F	~	30 ns

Times with ~2 meters of cable to ED, add ~20 ns per additional meter of cable to times A,C and E.

Fig. 4 Double hand-shake and typical times.

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Component side		Solder side
EO	- 1 -	$\overline{EO}$
ENFS	- 2 -	Return (-1,4 V)
C0	- 3 -	
C1	- 4 -	
C2	- 5 -	
C3	- 6 -	
S0	- 7 -	
S1	- 8 -	
S2	- 9 -	
S3	- 10 -	
S4	- 11 -	
SR	- 12 -	
ENCSE	- 13 -	
RT	- 14 -	
STROBE	- 15 -	
EIF	- 16 -	$\overline{EIF}$
F	- 17 -	Return (-1,4 V)
B4	- 18 -	
W0	- 19 -	
W1	- 20 -	
W2	- 21 -	
W3	- 22 -	
W4	- 23 -	
W5	- 24 -	
W6	- 25 -	
W7	- 26 -	
W8	- 27 -	
W9	- 28 -	
W10	- 29 -	
W11	- 30 -	
W12	- 31 -	
W13	- 32 -	
W14	- 33 -	
W15	- 34 -	
Free	- 35 -	GND

Fig. 5

Branch Input Connections (BI)
viewed from front panel

Signal		Return	
EO	• 1 •	$\overline{EO}$	Connector I1
ENFS	• 2 •	-1,4 V (from SE)	
C0	• 3 •		
C1	• 4 •		
C2	• 5 •		
C3	• 6 •		
S0	• 7 •		
S1	• 8 •		
S2	• 9 •		
S3	• 10 •		
S4	• 11 •		
SR	• 12 •		
Free	• 13 •		
Free	• 14 •		
ENCSE	• 15 •		
RT	• 16 •		
STROBE	• 17 •		
EIF	• 18 •	$\overline{EIF}$	
F	• 19 •	-1,4 V (from SE)	
B4	• 20 •		
Free	• 1 •	Free	Connector I2
Free	• 2 •	Free	
W0	• 3 •	-1,4 V (from SE)	
W1	• 4 •		
W2	• 5 •		
W3	• 6 •		
W4	• 7 •		
W5	• 8 •		
W6	• 9 •		
W7	• 10 •		
W8	• 11 •		
W9	• 12 •		
W10	• 13 •		
W11	• 14 •		
W12	• 15 •		
W13	• 16 •		
W14	• 17 •		
Free	• 18 •	Free	
W15	• 19 •	-1,4 V (from SE)	
Free	• 20 •		

Fig. 6

Internal Input Bus Connections (IIB)

viewed from component side

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Component side		Solder side
SIGNAL		$\overline{\text{SIGNAL}}$
Free	- 1 -	Free
"	- 2 -	"
"	- 3 -	"
"	- 4 -	"
"	- 5 -	"
"	- 6 -	"
START READ (SR)	- 7 -	$\overline{\text{START READ}}$ ($\overline{\text{SR}}$)
Free	- 8 -	Free
"	- 9 -	"
ENCODE (ENC)	- 10 -	$\overline{\text{ENCODE}}$ ($\overline{\text{ENC}}$)
Free	- 11 -	Free
"	- 12 -	"
RESET (RT)	- 13 -	$\overline{\text{RESET}}$ ($\overline{\text{RT}}$)
Free	- 14 -	Free
"	- 15 -	"
EOR	- 16 -	$\overline{\text{EOR}}$
DF	- 17 -	$\overline{\text{DF}}$
Free	- 18 -	Free
B0	- 19 -	$\overline{\text{B0}}$
B1	- 20 -	$\overline{\text{B1}}$
B2	- 21 -	$\overline{\text{B2}}$
B3	- 22 -	$\overline{\text{B3}}$
B4	- 23 -	$\overline{\text{B4}}$
B5	- 24 -	$\overline{\text{B5}}$
B6	- 25 -	$\overline{\text{B6}}$
B7	- 26 -	$\overline{\text{B7}}$
B8	- 27 -	$\overline{\text{B8}}$
B9	- 28 -	$\overline{\text{B9}}$
B10	- 29 -	$\overline{\text{B10}}$
B11	- 30 -	$\overline{\text{B11}}$
B12	- 31 -	$\overline{\text{B12}}$
B13	- 32 -	$\overline{\text{B13}}$
B14	- 33 -	$\overline{\text{B14}}$
B15	- 34 -	$\overline{\text{B15}}$
GROUND (GND)	- 35 -	GROUND (GND)

Fig. 7

Data Output Connector
viewed from front panel

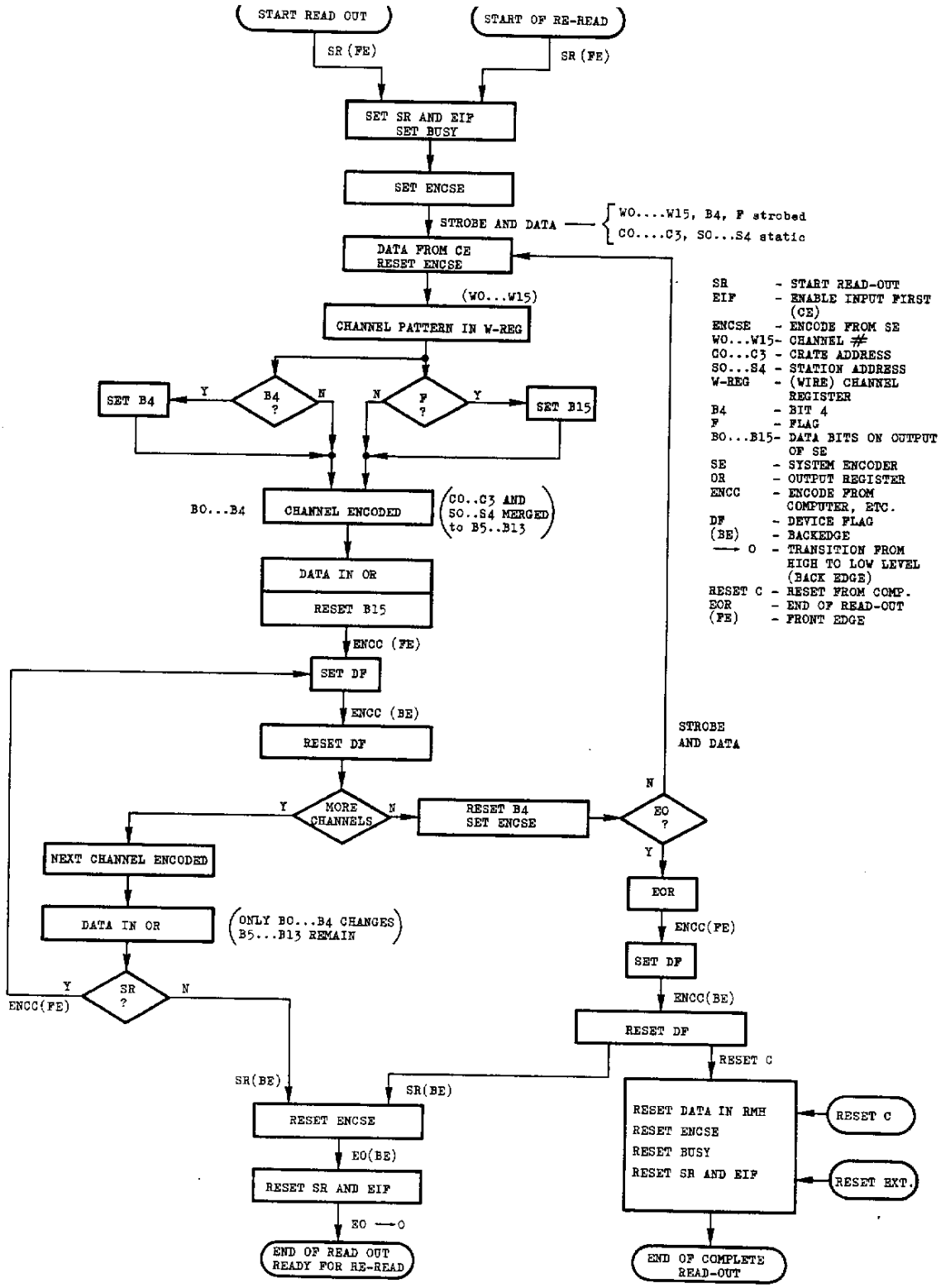
Signal				Return
ENC	-	1	-	Return (GND)
SR	-	2	-	" "
EOR	-	3	-	RT
DF	-	4	-	
B0	-	5	-	
B1	-	6	-	
B2	-	7	-	
B3	-	8	-	
B4	-	9	-	Return (GND)
B5	-	10	-	
B6	-	11	-	
B7	-	12	-	
B8	-	13	-	
B9	-	14	-	
B10	-	15	-	
B11	-	16	-	
B12	-	17	-	
B13	-	18	-	
B14	-	19	-	PAR
B15	-	20	-	Return (GND)

Fig. 8

Internal Output Bus Connections (IOB)
viewed from solder side

Component side		Solder side
Free	- 1 -	Free
"	- 2 -	"
"	- 3 -	"
"	- 4 -	"
"	- 5 -	"
		No contacts (connector cut-out)
Free	- 35 -	Free
"	- 36 -	"
"	- 37 -	"
"	- 38 -	-6 V
"	- 39 -	Free
-5,2 V	- 40 -	"
Free	- 41 -	"
-5,2 V	- 42 -	"
GND	- 43 -	GND

Fig. 9
Dataway Connections (CAMAC Connector)
viewed from front panel



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